Contoc Components GmbH & Co. KG
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LOW POWER PROGRAMMABLE OSCILLATOR

SERIES „CSO-1292“ 115.0—137.0 MHz

FEATURES

+ 100% pin-to-pin drop-in replacement to quartz-based XO
+ High Frequency Programmable Low Power Oscillator for Low Cost
+ Excellent long time reliability—outperforms quartz-based XO
+ Excellent total frequency stability as low as ±20 ppm over –40/+85°C
+ Excellent long term aging
+ Low power consumption of 4.8 mA typical
+ Programmable drive strength for improved jitter, system EMI reduction, or driving large capacitive loads
+ LVCMOS/HCMOS compatible output
+ Industry-standard packages: 2.0x1.6; 2.5x2.0; 3.2x2.5; 5.0x3.2; 7.0x5.0
+ Express samples within 1 day ex works
+ Pb-free, RoHS and REACH compliant / MSL1@260°C

APPLICATIONS

+ Ideal for GPON/GPON, network switches, routers. servers, embedded systems, Telecom, Medical, Industrial, Consumer, etc.
+ Ideal for Ethernet, PCI-E, DDR, USB, SATA, Storage server, etc.

GENERAL DATA[1]

PARAMETER AND CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
FREQUENCY RANGE						
Output Frequency Range	f	115	–	137	MHz	
FREQUENCY STABILITY AND AGING						
Frequency Stability	F_stab	-20	–	+20	PPM	Inclusive of initial tolerance at 25°C, 1st year aging at 25°C,
		-25	–	+25	PPM	and variations over operating temperature, rated power
		-50	–	+50	PPM	supply voltage and load.
OPERATING TEMPERATURE RANGE						
Operating Temperature Range	T_use	-20	–	+70	°C	Extended Commercial
		-40	–	+85	°C	Industrial
Storage Temperature Range	T_stor	-55	–	+125	°C	Storage
SUPPLY VOLTAGE AND CURRENT CONSUMPTION						
Supply Voltage	V_{DD}	1.62	1.8	1.98	V	Contact Contoc for 1.5V support
		2.25	2.5	2.75	V	
		2.52	2.8	3.08	V	
		2.7	3.0	3.3	V	
		2.97	3.3	3.63	V	
		2.25	–	3.63	V	
Current Consumption	I_{DD}	–	6.2	7.5	mA	No load condition, f = 125 MHz, V_{DD} = 2.8V, 3.0V, 3.3V, or 2.25V to 3.63V
	I_{DD}	–	5.4	6.4	mA	No load condition, f = 125 MHz, V_{DD} = 2.5V
	I_{DD}	–	4.8	5.6	mA	No load condition, f = 125 MHz, V_{DD} = 1.8V
OE Disable Current	I_OD	–	–	4	mA	V_{DD} = 2.5V to 3.3V, OE = GND, output is pulled down
		–	–	3.8	mA	V_{DD} = 1.8V, OE = GND, output is pulled down
Standby Current	I_std	–	2.6	4.3	µA	ST = GND, V_{DD} = 2.8V to 3.3V, output is pulled down
		–	1.4	2.5	µA	ST = GND, V_{DD}= 2.5V, output is pulled down
		–	0.6	1.3	µA	ST = GND, V_{DD} = 1.8V, output is pulled down

Note: 1. All electrical specifications in the above table are specified with 15 pF output load at default drive strength and for all V_{DD}(s) unless otherwise stated.

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GENERAL DATA[1] (continued)

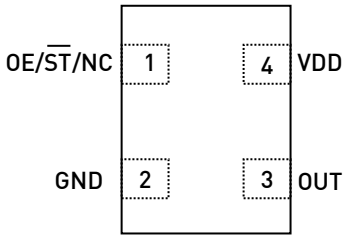
PARAMETER AND CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
LVCMOS OUTPUT CHARACTERISTICS						
Duty Cycle	DC	45	–	55	%	All V_{DD}s
Rise/Fall Time	Tr, Tf	–	1	2	ns	V_{DD} = 2.5V, 2.8V, 3.0V or 3.3V, 20% - 80%
		–	1.3	2.5	ns	V_{DD} =1.8V, 20% - 80%
		–	0.8	2	ns	V_{DD} = 2.25V - 3.63V, 20% - 80%
Output High Voltage	VOH	90%	–	–	V_{DD}	IOH = -4 mA (V_{DD} = 3.0V or 3.3V)
Output Low Voltage	VOL	–	–	10%	V_{DD}	IOL = 4 mA (V_{DD} = 3.0V or 3.3V)
INPUT CHARACTERISTICS						
Input High Voltage	VIH	70%	–	–	V_{DD}	Pin 1, OE or ST
Input Low Voltage	VIL	–	–	30%	V_{DD}	Pin 1, OE or ST
Input Pull-up Impedence	Z_in	–	87	100	kΩ	Pin 1, OE logic high or logic low, or ST logic high
		2	–	–	MΩ	Pin 1, ST logic low
STARTUP AND RESUME TIMING						
Startup Time	T_start	–	–	5	ms	Measured from the time V_{DD} reaches its rated minimum value
Enable/Disable Time	T_oe	–	–	130	ns	f = 115 MHz. For other frequencies, T_oe = 100 ns + 3* cycles
Resume Time	T_resume	–	–	5	ms	Measured from the time ST pin crosses 50% threshold
JITTER						
RMS Period Jitter	T_jitt	–	1.93	3	ps	f = 125 MHz, V_{DD} = 2.5V, 2.8V, 3.0V or 3.3V
		–	1.64	4	ps	f = 125 MHz, V_{DD} = 1.8V
RMS Phase Jitter (random)	T_phj	–	0.5	0.9	ps	Integration bandwidth = 900 kHz to 7.5 MHz
		–	1.3	2	ps	Integration bandwidth = 12 kHz to 20 MHz
EXCELLENT RELIABILITY DATA						
MTBF				500 million hours		
Shock Resistance:				10.000 g		
Vibration Resistance:				70 g		

Note: 1. All electrical specifications in the above table are specified with 15 pF output load and for all V_{DD}(s) unless otherwise stated.

PIN DESCRIPTION

PIN	SYMBOL		FUNCTIONALITY
1	OE/ST/NC	Output Enable	H or Open[2]: specified frequency output L: output is high impedance. Only output driver is disabled.
		Standby	H or Open[2]: specified frequency output L: output is low (weak pull down). Device goes to sleep mode. Supply current reduces to I_std.
		No Connect	Any voltage between 0 and V_{DD} or Open[2]: Specified frequency output. Pin 1 has no function.
2	GND	Power	Electrical ground[3]
3	OUT	Output	Oscillator output
4	V_{DD}	Power	Power supply voltage[3]

TOP VIEW



Note: 2. In OE or ST mode, a pull-up resistor of 10kΩ or less is recommended if pin 1 is not externally driven. If pin 1 needs to be left floating, use the NC option.
3. A capacitor value of 0.1 µF between V_{DD} and GND is recommended.

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TEST CIRCUIT AND WAVEFORM

FIGURE 1. TEST CIRCUIT

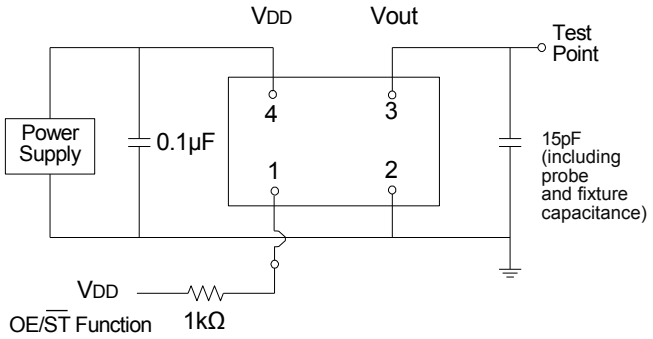
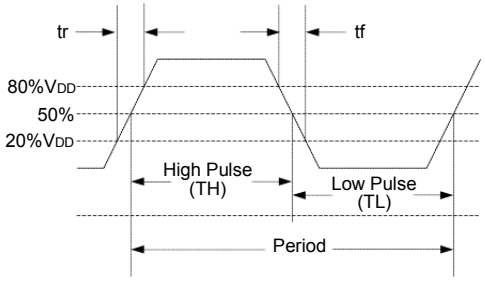
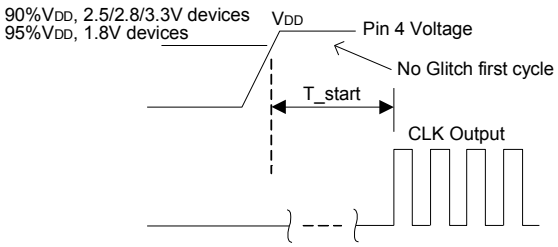


FIGURE 2. WAVEFORM



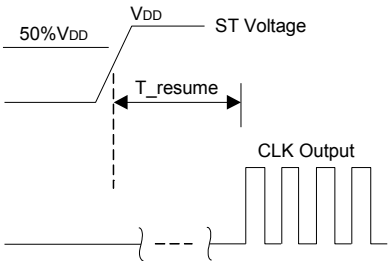
TIMING DIAGRAMS[4]

FIGURE 3. STARTUP TIMING (OE/ST MODE)



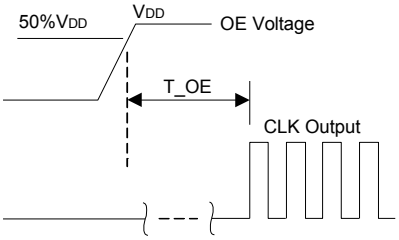
T_start: Time to start from power-off

FIGURE 4. STANDBY RESUME TIMING (ST MODE ONLY)



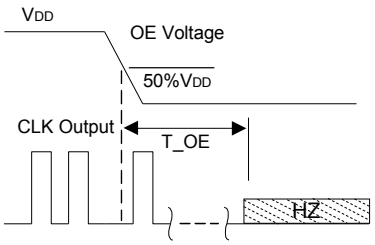
T_resume: Time to resume from ST

FIGURE 5. OE ENABLE TIMING (OE MODE ONLY)



T_OE: Time to re-enable the clock output

FIGURE 6. OE DISABLE TIMING (OE MODE ONLY)



T_OE: Time to put the output drive in High Z mode

Note: 4. CSO-1292 supports no runt pulses and no glitches during startup or resume.

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PERFORMANCE PLOTS[5]

FIGURE 7. IDD vs. FREQUENCY

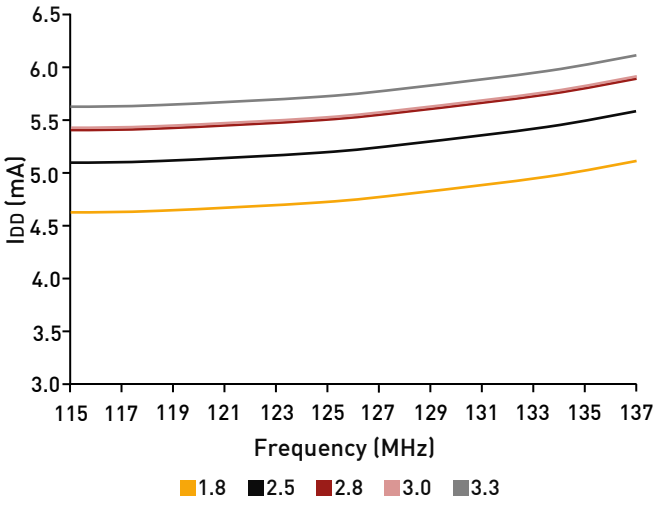


FIGURE 8. RMS PERIOD JITTER vs. FREQUENCY

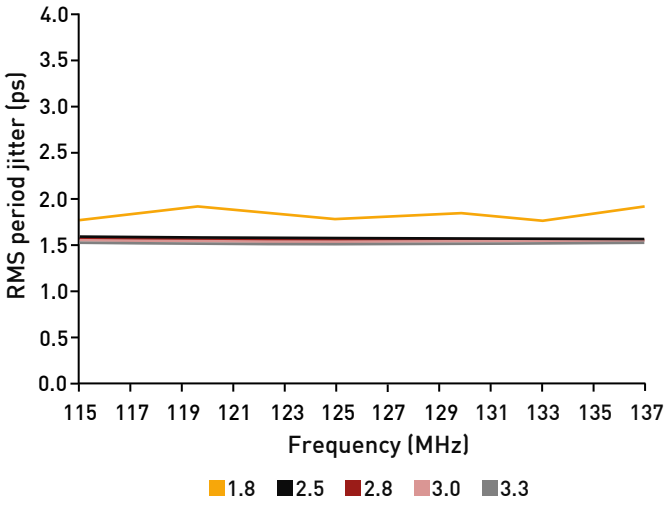


FIGURE 9. RMS PHASE JITTER vs. FREQUENCY

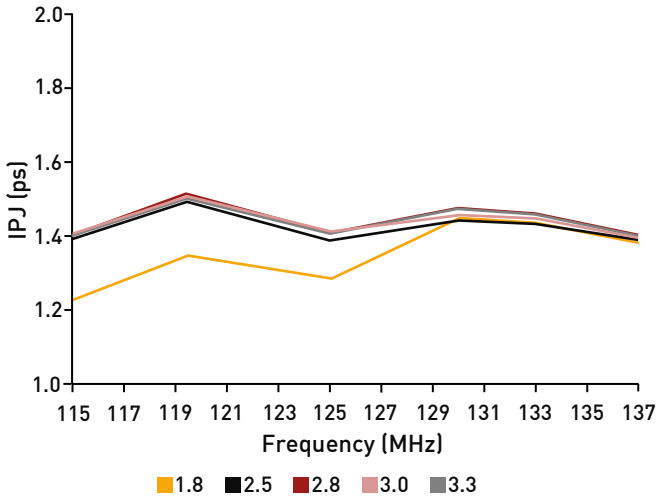


FIGURE 10. RMS PHASE JITTER vs. FREQUENCY

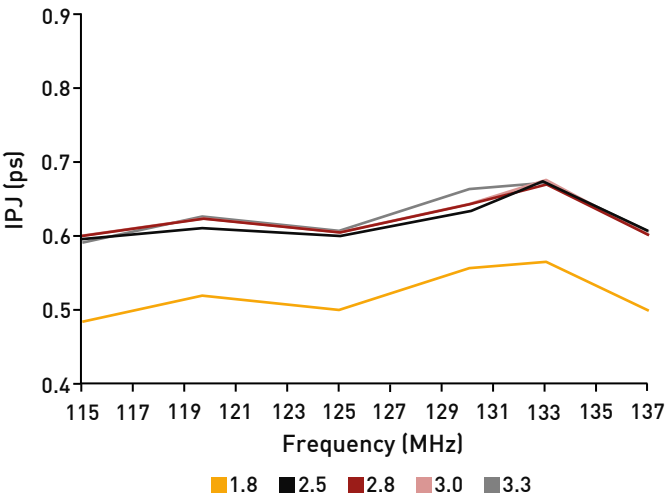


FIGURE 11. DUTY CYCLE vs. FREQUENCY

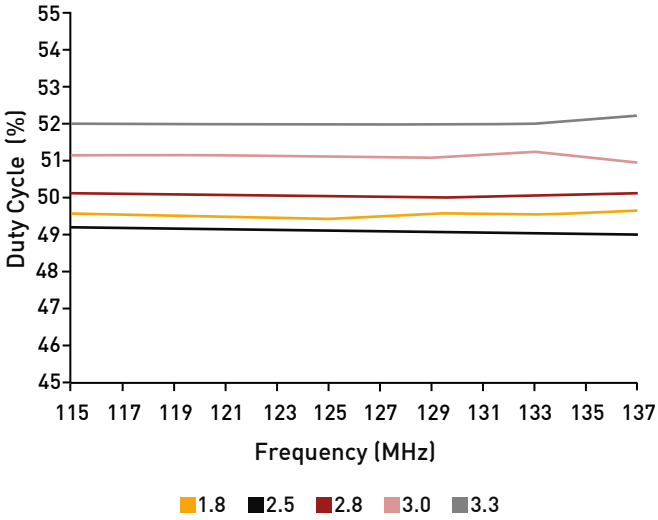
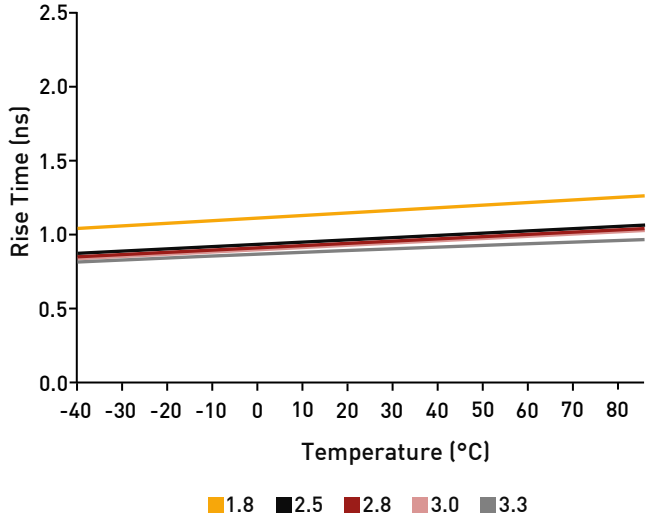


FIGURE 12. RISE TIME vs. TEMPERATURE, 125 MHZ OUTPUT



Note: 5. All plots are measured with 15 pF load at room temperature, unless otherwise stated.

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PROGRAMMABLE DRIVE STRENGTH

The CSO-1292 includes a programmable drive strength feature to provide a simple, flexible tool to optimize the clock rise/fall time for specific applications. Benefits from the programmable drive strength feature are:

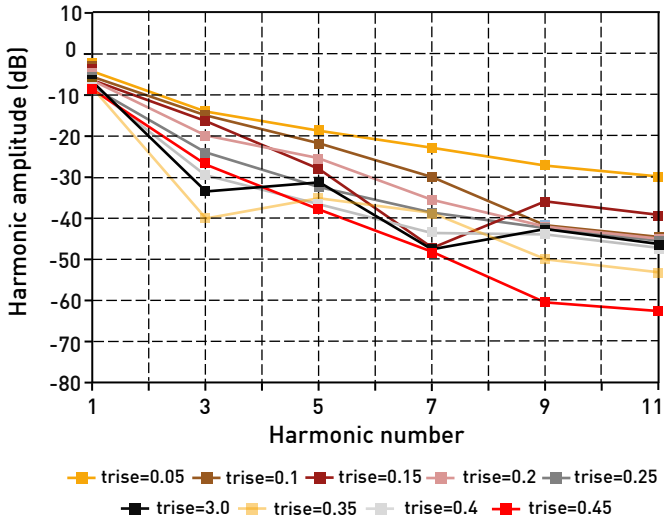
+ Improves system radiated electromagnetic interference (EMI) by slowing down the clock rise/fall time
+ Improves the downstream clock receiver's (RX) jitter by decreasing (speeding up) the clock rise/fall time.
+ Ability to drive large capacitive loads while maintaining full swing with sharp edge rates.

For more detailed information about rise/fall time control and drive strength selection, see the Contoc Applications Note section: http://www.contoc.com

EMI REDUCTION BY SLOWING RISE/FALL TIME

Figure 13 shows the harmonic power reduction as the rise/fall times are increased (slowed down). The rise/fall times are expressed as a ratio of the clock period. For the ratio of 0.05, the signal is very close to a square wave. For the ratio of 0.45, the rise/fall times are very close to near-triangular waveform. These results, for example, show that the 11th clock harmonic can be reduced by 35 dB if the rise/fall edge is increased from 5% of the period to 45% of the period.

FIGURE 13. HARMONIC EMI REDUCTION AS A FUNCTION OF SLOWER RISE/FALL TIME



JITTER REDUCTION WITH FASTER RISE/FALL TIME

Power supply noise can be a source of jitter for the downstream chipset. One way to reduce this jitter is to increase rise/fall time (edge rate) of the input clock. Some chipsets would require faster rise/fall time in order to reduce their sensitivity to this type of jitter. The CSO-1292 provides up to 3 additional high drive strength settings for very fast rise/fall time. Refer to the Rise/Fall Time Tables to determine the proper drive strength.

HIGH OUTPUT LOAD CAPABILITY

The rise/fall time of the input clock varies as a function of the actual capacitive load the clock drives. At any given drive strength, the rise/fall time becomes slower as the output load increases. As an example, for a 3.3V CSO-1292 device with default drive strength setting, the typical rise/fall time is 1ns for 15 pF output load. The typical rise/fall time slows down to 1.8ns when the output load increases to 30 pF. One can choose to speed up the rise/fall time to 1.38ns by then increasing the drive strength setting on the CSO-1292.
The CSO-1292 can support up to 30 pF or higher in maximum capacitive loads with up to 3 additional drive strength settings. Refer to the Rise/Tall Time Tables to determine the proper drive strength for the desired combination of output load vs. rise/fall time.

CSO-1292 DRIVE STRENGTH SELECTION

Tables 1 through 5 define the rise/fall time for a given capacitive load and supply voltage.

1. Select the table that matches the CSO-1292 nominal supply voltage (1.8V, 2.5V, 2.8V, 3.0V, 3.3V).
2. Select the capacitive load column that matches the application requirement (5 pF to 30 pF)
3. Under the capacitive load column, select the desired rise/fall times.
4. The left-most column represents the part number code for the corresponding drive strength.
5. Add the drive strength code to the part number for ordering purposes.

CALCULATING MAXIMUM FREQUENCY

Based on the rise and fall time data given in Tables 1 through 5, the maximum frequency the oscillator can operate with guaranteed full swing of the output voltage over temperature as follows:

$$\text{Max. frequency} = \frac{1}{6 \times (\text{Trise})}$$

EXAMPLE 1

Calculate f_{MAX} for the following condition:

+ V_{DD} = 3.3V (Table 1)
+ Capacitive Load: 30pF
+ Desired Tr/Tf time = 2ns (rise/fall time part number code=U)

Part number for the above example:

CSO-1292-33-2520-E-25-M-125.000MHz-T-U

Drive strength code is inserted here. Standard setting is "S"

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RISE/FALL TIME (20% TO 80%) vs C_{LOAD}

TABLE 1. VDD = 1.8V RISE/FALL TIMES FOR SPECIFIC C_{LOAD}

RISE/FALL TIME TYP (NS)		
Drive Strength \ C_{LOAD}	5 pF	15 pF
T	0.93	n/a[6]
E	0.78	n/a
U	0.70	1.48
F or "-": standard	0.65	1.30

TABLE 2. VDD = 2.5V RISE/FALL TIMES FOR SPECIFIC C_{LOAD}

RISE/FALL TIME TYP (NS)		
Drive Strength \ C_{LOAD}	5 pF	15 pF
R	1.45	n/a
B	1.09	n/a
T	0.62	1.28
E or "-": standard	0.54	1.00
U	0.43	0.96
F	0.34	0.88

TABLE 3. VDD = 2.8V RISE/FALL TIMES FOR SPECIFIC C_{LOAD}

RISE/FALL TIME TYP (NS)			
Drive Strength \ C_{LOAD}	5 pF	15 pF	30 pF
R	1.29	n/a	n/a
B	0.97	n/a	n/a
T	0.55	1.12	n/a
E or "-": standard	0.44	1.00	n/a
U	0.34	0.88	n/a
F	0.29	0.81	1.48

TABLE 4. VDD = 3.0V RISE/FALL TIMES FOR SPECIFIC C_{LOAD}

RISE/FALL TIME TYP (NS)			
Drive Strength \ C_{LOAD}	5 pF	15 pF	30 pF
R	1.22	n/a	n/a
B	0.89	n/a	n/a
Tor "-": standard	0.51	1.00	n/a
E	0.38	0.92	n/a
U	0.30	0.83	n/a
F	0.27	0.76	1.39

TABLE 5. VDD = 3.3V RISE/FALL TIMES FOR SPECIFIC C_{LOAD}

RISE/FALL TIME TYP (NS)			
Drive Strength \ C_{LOAD}	5 pF	15 pF	30 pF
R	1.16	n/a	n/a
B	0.81	n/a	n/a
T or "-": standard	0.46	1.00	n/a
E	0.33	0.87	n/a
U	0.28	0.79	1.46
F	0.25	0.72	1.31

Note: 6. "n/a" indicates that the resulting rise/fall time from the respective combination of the drive strength and output load does not provide rail-to-rail swing and is not available

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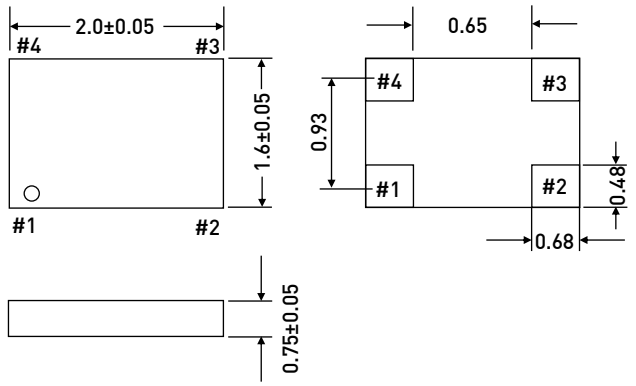
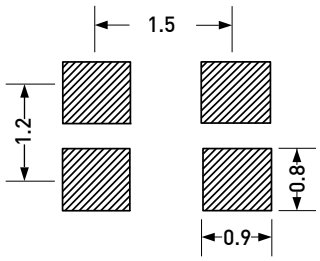
DIMENSIONS AND PATTERNS

PACKAGE SIZE – DIMENSIONS (UNIT:MM)

2.0 X 1.6 X 0.75 MM

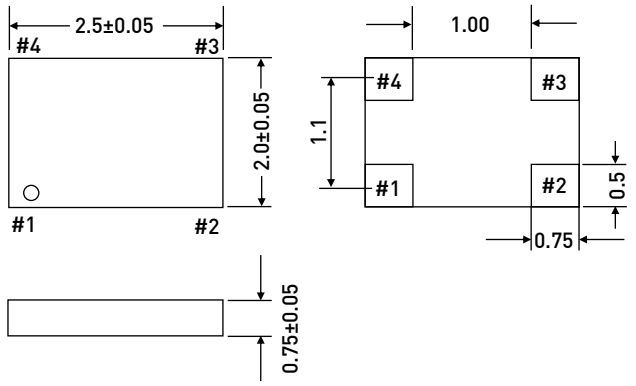


RECOMMENDED LAND PATTERN (UNIT:MM) [7]

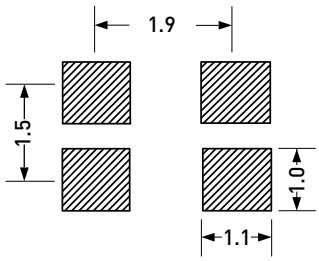


PACKAGE SIZE – DIMENSIONS (UNIT:MM)

2.5 X 2.0 X 0.75 MM

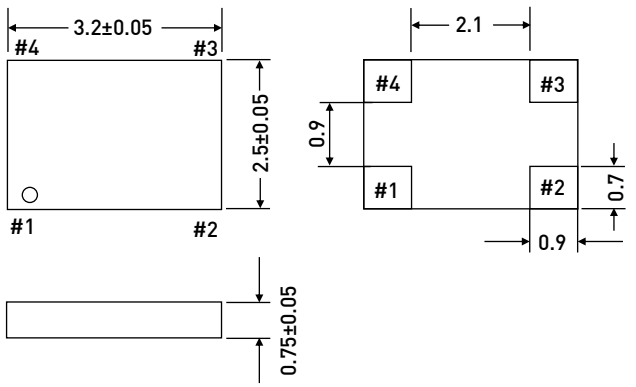


RECOMMENDED LAND PATTERN (UNIT:MM)

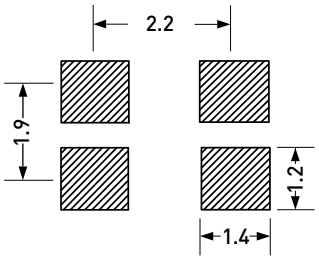


PACKAGE SIZE – DIMENSIONS (UNIT:MM)

3.2 X 2.5 X 0.75 MM



RECOMMENDED LAND PATTERN (UNIT:MM)



Note: 7. A capacitor value of 0.1 µF between V_{DD} and GND is recommended (see note 2 + 3).

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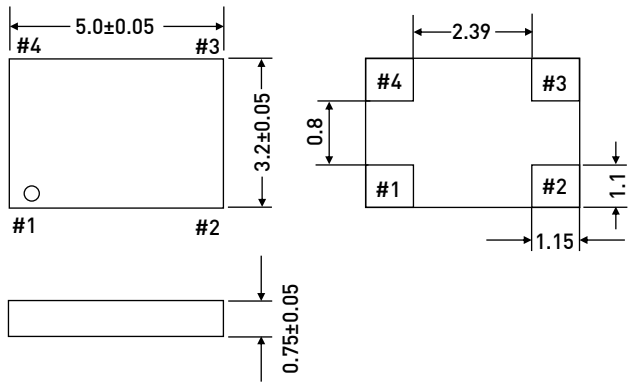
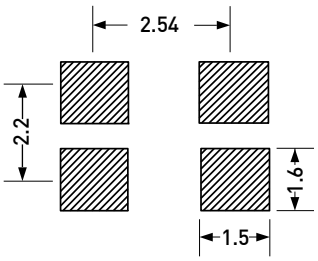
DIMENSIONS AND PATTERNS

PACKAGE SIZE – DIMENSIONS (UNIT:MM)

5.0 X 3.2 X 0.75 MM

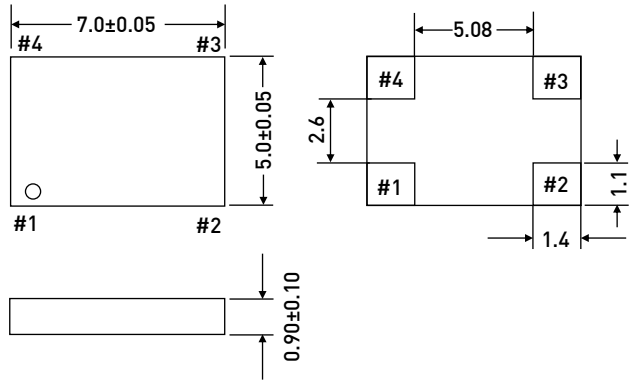


RECOMMENDED LAND PATTERN (UNIT:MM) [8]

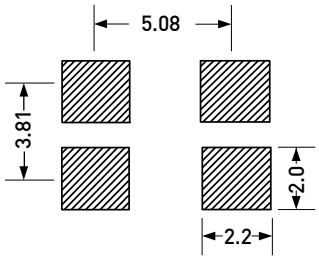


PACKAGE SIZE – DIMENSIONS (UNIT:MM)

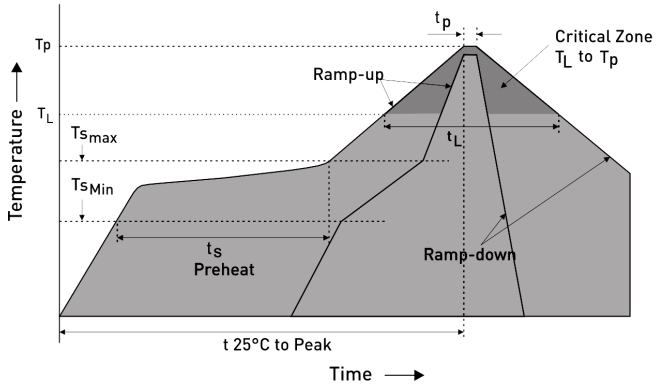
7.0 X 5.0 X 0.90 MM



RECOMMENDED LAND PATTERN (UNIT:MM)



REFLOW SOLDER PROFILE



IPC/JEDEC Standard	IPC/JEDEC J-STD-020
Moisture Sensitivity Level	Level 1
TS MAX to TL (Ramp-up Rate)	3°C/second Maximum
Preheat	
- Temperature Minimum (TS MIN)	150°C
- Temperature Typical (TS TYP)	175°C
- Temperature Typical (TS MAX)	200°C
- Time (tS)	60 - 180 Seconds
Ramp-up Rate (TL to TP)	3°C/second Maximum
Time Maintained Above:	
- Temperature (TL)	217°C
- Time (TL)	60 - 150 Seconds
Peak Temperature (TP)	260°C Maximum
Target Peak Temperature (TP Target)	255°C
Time within 5°C of actual peak (tP)	20 -40 Seconds
Max. Number of Reflow Cycles	3
Ramp-down Rate	6°C/second Maximum
Time 25°C to Peak Temperature (t)	8 minutes Maximum

Note: 8. A capacitor value of 0.1 µF between V_{DD} and GND is recommended (see note 2 + 3).

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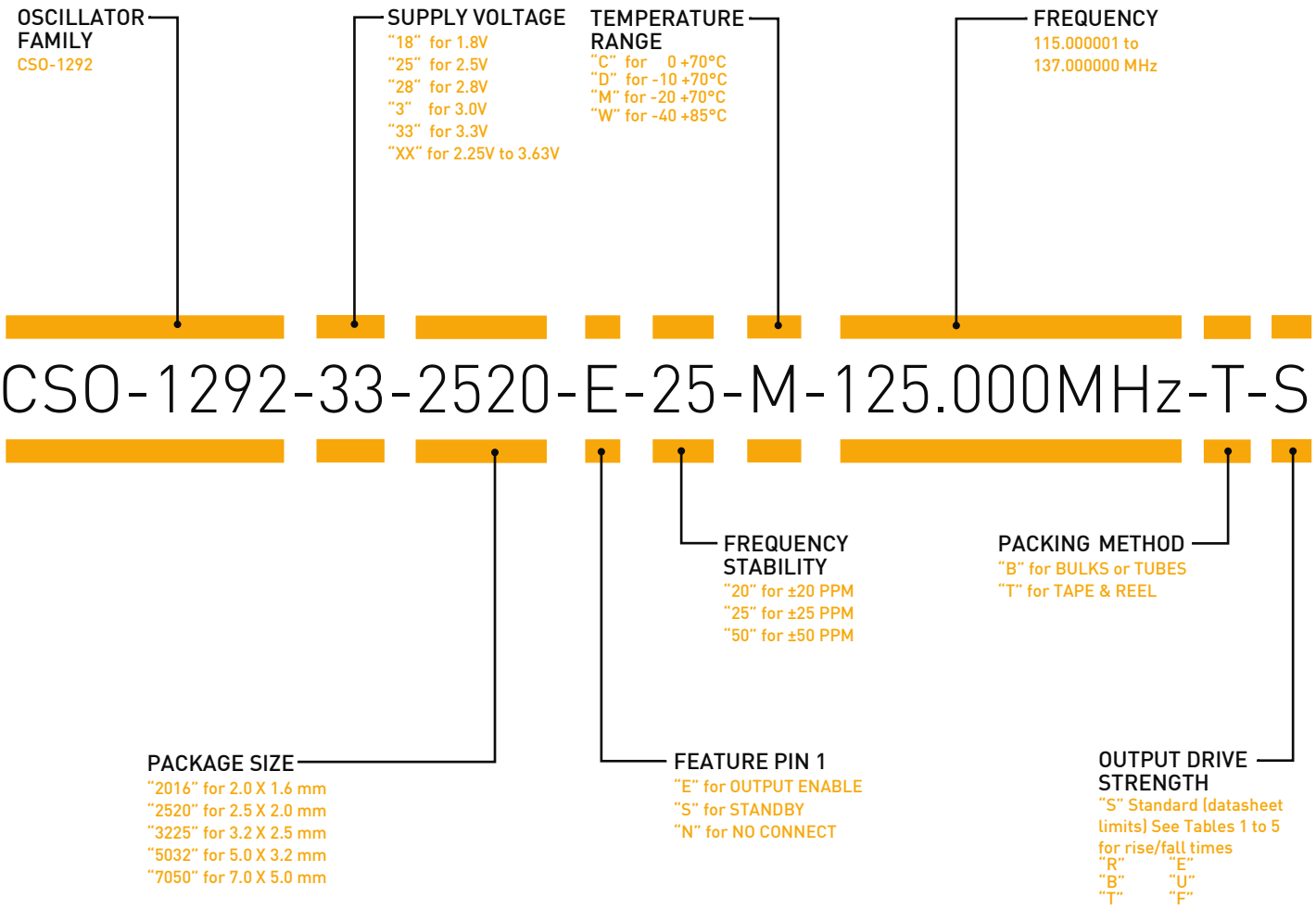
ORDERING INFORMATION



EXAMPLE: CSO-1292-33-2520-E-25-M-125.000MHz-T-S

PLEASE INDICATE YOUR REQUIRED PARAMETERS

EXPRESS SAMPLES ARE DELIVERABLE ON THE SAME DAY IF ORDERED UNTIL 02:00 PM!

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DMSZ
certified according to
ISO 9001
QM 00886

OUR COMPANY IS CERTIFIED ACCORDING TO ISO 9001:2008 IN OCTOBER 2013 BY THE DMSZ CERTIFIKATION GMBH.

THIS IS FOR YOU TO ENSURE THAT THE PRINCIPLES OF QUALITY MANAGEMENT ARE FULLY IMPLEMENTED IN OUR QUALITY MANAGEMENT SYSTEM AND QUALITY CONTROL METHODS ALSO DOMINATE OUR QUALITY STANDARDS.